

## **DEVICE FOR CONTROLLING A VOLTAGE-CONTROLLED POWER SWITCH**

### **Background Of The Invention**

5

#### **1. Field of the Invention**

The present invention relates to the control of voltage-controlled switches, and especially the control of power switches.

#### **10 2. Discussion of the Related Art**

When a control voltage capable of making a voltage-controlled switch operate in a desired conduction state is abruptly applied to said switch, an overcurrent tends to occur in the switch at the turning-on. In particular, in the case of a power switch connected to an inductive load such as an electric motor winding capable of causing 15 voltages on the order of several tens of volts, the overcurrent is likely to damage the switch. To avoid this problem, power switch control devices varying the voltage by stages have been provided. In the case where the power circuit is for example a motor control circuit operating on the mains, and where the power switch is an IGBT or MOS power transistor, the control circuit must provide high voltages and conduct high 20 currents, and no control integrated device of such power switches is currently known.

### **Summary Of The Invention**

An object of the present invention is to provide an integrated and inexpensive device for controlling a voltage-controlled power switch.

25 To achieve this and other objects, the present invention provides a control device comprising a circuit for setting to the high state and/or a circuit for setting to the low state.

More specifically, the present invention provides a device for controlling a 30 voltage-controlled switch, comprising two circuits respectively for setting to the high level and for setting to the low level a control terminal of the voltage-controlled switch; one at least of said circuits comprising a power transistor capable of connecting the control terminal to a high, respectively low voltage; a bipolar control transistor having its emitter, respectively its collector, connected to the control terminal of the power

transistor, the base of the control transistor being likely to receive a control current; a first diode having its cathode, respectively, its anode, connected to a first predetermined voltage smaller than the high voltage, and having its anode, respectively its cathode, connected to the base of the control transistor.

5 According to an embodiment of the present invention, said at least one of said circuits is the circuit for setting to the high level and it comprises a first output terminal capable of being connected to the control terminal of the voltage-controlled switch; the power and control transistors being first and second NPN-type bipolar transistors forming a Darlington assembly arranged between the first output terminal and the high 10 voltage; the anode of the first diode being connected to the base of the control transistor via a first controllable circuit breaker; and the device being capable of being connected to a control block successively enabling:

a/ applying the control current to the Darlington assembly and turning on the first circuit breaker; and  
15 b/ after a first predetermined duration, turning off the first circuit breaker.

According to an embodiment of the present invention, the device further comprises first and second P-channel MOS transistors having their sources connected to the high voltage, a controllable current source being connected to the drain of the first MOS transistor, the gates of the first and second MOS transistors being connected to the 20 drain of the first MOS transistor and the drain of the second MOS transistor being connected to the base of the control transistor and to the drain of a third N-channel MOS transistor, having its source connected to a low supply voltage and the gate of which is capable of being connected to the control block via a second controllable circuit breaker, a second diode having its cathode and its anode respectively connected to the drain of the 25 third MOS transistor and to the first output terminal.

According to an embodiment of the present invention, the first circuit breaker comprises a fourth P-channel MOS transistor having its source connected to the base of the control transistor and having its drain connected to the anode of the first diode, the gate of the fourth MOS transistor being connected via a third resistor to the drain of a 30 fifth P-channel MOS transistor, the source of the fifth MOS transistor being connected to the high voltage, the gate of the fifth MOS transistor being connected to the gate of the first MOS transistor, the gate of the fourth MOS transistor being also connected: to the

anode of a first zener diode having its cathode connected to the anode of a second zener diode having its cathode connected to the base of the control transistor; to the anode of a third diode having its cathode connected to the base of the control transistor; and to the cathode of a fourth diode having its anode connected to the drain of the fifth MOS transistor; a fifth diode having its anode connected to the drain of the fifth MOS transistor and its cathode connected to the drain of a sixth N-channel MOS transistor having its source connected to a ground voltage and the gate of which is capable of being connected to the control block.

According to an embodiment of the present invention, the second circuit breaker 10 comprises a buffer circuit having an input terminal, an output terminal, and a control terminal, the output terminal of which can take three states: 1 or 0 according to whether the input terminal is at 1 or 0 when the control terminal is at 1, and a high-impedance state if the control terminal is at 0.

According to an embodiment of the present invention, the device's circuit for 15 setting to the low level comprises a second output terminal capable of being connected to the control terminal of the voltage-controlled switch and comprising: a seventh N-channel MOS transistor arranged between the second output terminal and the low voltage, and the gate of which is capable of being connected to the control block via the second controllable circuit breaker; and a limiting means controllable for, when the 20 second circuit breaker is off, providing the gate of the seventh MOS transistor with an activation voltage as long as the voltage of the second output terminal is greater than a predetermined voltage ranging between the high and ground voltages; the control block enabling, upon activation of the Darlington assembly, provision of a deactivation signal to the gate of the seventh MOS transistor and, a second predetermined duration after the 25 turning-off of the first circuit breaker:

c/ deactivation the Darlington assembly and turning off the second circuit breaker; and

d/ after a third predetermined duration, turning on the second circuit breaker and providing an activation signal to the gate of the seventh MOS transistor.

According to an embodiment of the present invention, the limiting means 30 comprises a third bipolar transistor arranged between the second output terminal and the gate of the seventh MOS transistor, and a sixth diode capable of canceling the base

current of the third bipolar transistor when the voltage of the second output terminal is smaller than the second predetermined voltage.

According to an embodiment of the present invention, the collector of the third bipolar transistor is connected via a fourth resistor to the gate of the seventh MOS transistor, a fifth resistor connecting the gate of the seventh MOS transistor to the low voltage, the base of the third bipolar transistor being connected to the cathode of the sixth diode, having its anode connected to the second predetermined voltage, the base of the third bipolar transistor being also connected via a sixth resistor to the drain of an eighth N-type MOS transistor, having its source connected to the ground voltage and the gate of which is capable of being connected to the control block.

The present invention also aims at a control device in which said at least one of said circuits is the circuit for setting to the low level and comprises a first output terminal capable of being connected to the control terminal of the voltage-controlled switch; the power transistor being an N-channel MOS transistor and the control transistor being a PNP-type bipolar transistor having its emitter and its collector respectively connected to the drain and to the gate of the power transistor, the gate of the power transistor being further connected to the low voltage via a resistor and connected via a first controllable circuit breaker to a control terminal of the power transistor; the device being capable of being connected to a control block enabling:

a/ deactivating the circuit for setting to the high level, turning off the first circuit breaker, and applying the control current of the control transistor; and

b/ after a first predetermined duration, deactivating the control current of the control transistor, turning on the first circuit breaker, and providing an activation signal to the gate of the power transistor.

According to an embodiment of the present invention, the circuit for setting to the high level comprises: a second output terminal capable of being connected to the control terminal of the voltage-controlled switch; a Darlington assembly arranged between the second output terminal and the high voltage, a control terminal of the Darlington assembly being likely to receive a control current; and a second diode having its cathode connected to a second predetermined voltage smaller than the high voltage and its anode connected to the control terminal of the Darlington assembly via a second controllable circuit breaker; the control block enabling successively:

- c/ providing a deactivation signal to the gate of the power transistor, applying the control current of the Darlington assembly, and turning on the second circuit breaker; and
- d/ after a second predetermined duration, turning off the second circuit breaker.

5

### Brief Description Of The Drawings

The foregoing objects, features, and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Fig. 1 schematically shows an IGBT control device according to the present invention;

Fig. 2 illustrates the operation of the device of Fig. 1; and

Fig. 3 shows in detailed fashion an embodiment of controllable circuit breakers of Fig. 1.

15

### Detailed Description

The same elements have been designated with the same reference numerals in the different drawings. Only those elements necessary to the understanding of the present invention have been shown.

An embodiment of the present invention will be described in the case where the voltage-controlled power switch is an insulated-gate bipolar transistor or IGBT. The present invention aims at a device for controlling a voltage-controlled switch, comprising two circuits (1, 17) respectively for setting to the high level and for setting to the low level a control terminal of the voltage-controlled switch.

Fig. 1 schematically shows an embodiment of an IGBT control device according to the present invention, of which circuit 1 for setting to the high level comprises a first output terminal OUTh capable of being connected to the gate of an IGBT not shown. Circuit 1 comprises a power transistor 2 connected between a high supply voltage Vh and terminal OUTh and a control circuit for providing an activation signal to transistor 2. Circuit 1 also comprises a circuit activable to cancel the activation signal of transistor 2 when the voltage of terminal OUTh exceeds a voltage Von smaller than voltage Vh.

According to a feature of the present invention, power transistor 2 is an NPN-type bipolar transistor and the control circuit of transistor 2 comprises an NPN-type bipolar

transistor 3. Transistors 2 and 3 form a Darlington assembly: their collectors are connected to voltage  $V_h$  and their emitters are preferably connected to terminal  $OUT_h$ , each by a resistor. The base of NPN power transistor 3 is connected to the emitter of NPN power transistor 2. The base of NPN control transistor 3 forms the control terminal 5 of the Darlington assembly.

The control circuit of transistor 2 further comprises two P-channel MOS transistors 4 and 6 assembled as a current mirror, having their sources connected to voltage  $V_h$ . The respective drains of transistors 4 and 6 are connected to a current source 8 controllable in all or nothing and to the control terminal of the Darlington assembly. 10 The respective sizes of transistors 4 and 6 are selected for transistor 4 to consume a small current and for the current provided by transistor 6 to enable fast activation of the Darlington assembly. The control terminal of the Darlington assembly is also connected to the drain of an N-channel MOS transistor 10, having its source connected to a low supply voltage  $V_l$ . The gate of transistor 10 is connected to a control terminal 12 via a 15 controllable circuit breaker 14. An embodiment of circuit breaker 14 is described hereafter in relation with Fig. 3.

According to a feature of the present invention, the circuit for canceling the activation signal of transistor 2 comprises a diode D1 having its anode connected to the control terminal of the Darlington assembly via a controllable circuit breaker 16. The 20 cathode of diode D1 is connected to a predetermined voltage  $V_{on}$ . An embodiment of circuit breaker 16 is described hereafter in relation with Fig. 3.

Current source 8, control terminal 12, and circuit breakers 14 and 16 are capable of being connected to a control block 30. Control block 30 may be integrated with the control device or on a separate chip, as shown by the dotted lines.

25 Fig. 2 illustrates the operation of circuit 1 for setting to the high level. Signals S8, S12, S14, and S16 respectively show the signals provided to elements 8, 12, 14, and 16. Fig. 2 also shows voltage  $V_{out}$  of terminal  $OUT_h$ . It is considered that initially, current source 8 is deactivated, that control terminal 12 is at a voltage capable of activating transistor 10, and that circuit breakers 14 and 16 are respectively on and off 30 (which is represented herein with signals S8, S12, S14, and S16 respectively at 0, 1, 1, 0). The activation of transistor 10 maintains voltage  $V_{out}$  substantially at voltage  $V_l$ .

At a time  $t_0$ , block 30 activates current source 8, turns on circuit breaker 16, and

brings control terminal 12 to a voltage capable of deactivating transistor 10. Current source 8 conducts a current  $I_S$ , whereby a current  $I_M$  of fixed value is provided to the control terminal of the Darlington assembly. Current  $I_M$  activates the Darlington assembly and draws output terminal OUTh towards voltage  $V_h$ . The voltage of the 5 control terminal of the Darlington assembly is substantially equal to the voltage of output terminal OUTh (the output voltage plus two diode threshold voltages).

At a time  $t_0 + \delta t$ , corresponding to the time when the voltage of the control terminal of the Darlington assembly exceeds a value equal to voltage  $V_{on}$  plus the threshold voltage of diode D1, diode D1 turns on. For simplicity, it is considered 10 hereafter that time  $t_0 + \delta t$  corresponds to a time when the voltage of terminal OUTh is substantially equal to voltage  $V_{on}$ . Diode D1 is selected so that its turning-on diverts from the control terminal of the Darlington assembly a portion of current  $I_M$  sufficient to deactivate the Darlington assembly. The capacitor formed by the IGBT gate then remains substantially at voltage  $V_{on}$ . In practice, transistors 4 and 6 and the Darlington 15 assembly are selected for voltage  $V_{out}$  to increase fast, and times  $t_0$  and  $t_0 + \delta t$  are very close.

At a time  $t_1$ , a predetermined duration after time  $t_0$ , block 30 turns off circuit breaker 16. Current  $I_M$ , which can then no longer run through diode D1, activates back the Darlington assembly which brings terminal OUTh to a voltage substantially equal to 20 voltage  $V_h$ . The IGBT is then completely activated.

The control device according to the present invention thus enables providing an increasing voltage  $V_{out}$  between  $V_l$  and  $V_h$ , with a stage at a predetermined voltage  $V_{on}$  for a controllable duration  $t_1 - t_0$ .

To activate the IGBT, voltage  $V_{out}$  must be decreased from voltage  $V_h$  to voltage 25  $V_l$ . It is for this purpose possible to control block 30 to deactivate current source 8 and activate transistor 10, but voltage  $V_{out}$  then decreases without stopping at a stage.

The present invention also provides that the control device can comprise a specific circuit 17 for setting to the low level to decrease voltage  $V_{out}$  with a stop at a stage.

30 As shown in Fig. 1, an embodiment of circuit 17 for setting to the low level comprises a second output terminal OUTl capable of being connected to the IGBT gate. In practice, terminals OUTh and OUTl may be connected together directly to the IGBT

gate, or be connected to the IGBT gate via a resistive bridge. Circuit 17 comprises a power transistor 18 connected to voltage  $V_l$ , and capable of decreasing the voltage of terminal OUTl. According to the present invention, power transistor 18 is controllable either by a circuit enabling decreasing the voltage of terminal OUTl from voltage  $V_h$  to a 5 voltage  $V_{off}$  ranging between  $V_h$  and GND, or by control block 30 to decrease the voltage of terminal OUTl from voltage  $V_{off}$  to voltage  $V_l$ .

According to a feature of the present invention, power transistor 18 is an N-channel MOS transistor 18 having its drain connected to output terminal OUTl and its source connected to voltage  $V_l$ . The gate of transistor 18 is connected to control terminal 10 12 via circuit breaker 14.

According to a feature of the present invention, the circuit enabling bringing terminal OUTl to voltage  $V_{off}$  comprises a PNP-type bipolar control transistor 20 having its emitter connected to output terminal OUTl, and having its collector connected via a resistor 22 to the gate of transistor 18. A resistor 24 connects the gate of transistor 18 to voltage  $V_l$ . The base of transistor 20 is connected to the cathode of a diode D2 having its 15 anode connected to predetermined voltage  $V_{off}$ . The base of transistor 20 is also connected via a resistor 26 to the drain of an N-type MOS transistor 28, having its source connected to a ground voltage GND. A protection diode 32 has its cathode and anode respectively connected to the control terminal of the Darlington assembly and to terminal 20 OUTh. The gate of transistor 28 is capable of being connected to control block 30.

Fig. 2 illustrates the operation of circuit 17 for setting to the low level by means of preceding signals S8, S12, S14, and S16 and of a signal S28 representing the signal provided by block 30 to the gate of transistor 28. Transistor 28 is initially deactivated. It is considered in Fig. 2 that terminals OUTh and OUTl are connected together and that 25 they are at the same voltage  $V_{out}$ .

At a time  $t_2$  when the IGBT is desired to be activated, block 30 deactivates current source 8, turns off circuit breaker 14, and activates transistor 28 by bringing signal S28 from 0 to 1. The deactivation of current source 8 switches off current  $I_m$  and deactivates the Darlington assembly. A current then flows from terminal OUTl to ground GND through emitter/base junction transistor 20, then through resistor 26 and through transistor 28. The base current of transistor 20 activates transistor 20, and creates a collector current which raises the gate voltage of transistor 18. Transistor 20 30

and resistors 22, 24 are chosen so that transistor 18 is then activated and draws output terminal OUT1 towards voltage VI. The base voltage of transistor 20 is equal to the voltage of output terminal OUT1 minus the base-emitter voltage of transistor 20.

At a time  $t_2 + \delta t'$ , corresponding to the time when the base voltage of transistor 20 falls below a value equal to voltage  $V_{off}$  minus threshold voltage  $V_s$  of diode D2, diode D2 turns on. The on state of diode D2 maintains the base of transistor 20 at voltage  $V_{off} - V_s$  while the voltage of terminal OUT1 keeps on decreasing. When the voltage of terminal OUT1 minus the base-emitter voltage of transistor 20 is smaller than voltage  $V_{off} - V_s$ , the base-emitter junction of transistor 20 blocks and transistor 20 is deactivated.

10 The gate voltage of transistor 18 drops, which deactivates transistor 18. For simplicity, it is considered hereafter that time  $t_2 + \delta t'$  corresponds to a time when the voltage of terminal OUT1, substantially equal to voltage  $V_{off}$ , stops decreasing. The capacitor formed by the IGBT gate then substantially remains at voltage  $V_{off}$ . In practice, transistors 18 and 20 and resistors 22, 24 are selected for voltage  $V_{out}$  to decrease fast, 15 and times  $t_2$  and  $t_2 + \delta t'$  are very close.

At a time  $t_3$ , a predetermined time after time  $t_2$ , block 30 turns on circuit breaker 14, deactivates transistor 28, and brings control terminal 12 to a voltage capable of activating transistors 10 and 18. The activation of transistors 10 and 18 lowers voltage  $V_{out}$  to voltage VI.

20 The voltage of the output terminal of the device according to an embodiment of the present invention thus decreases between  $V_h$  and VI, with a stage at a predetermined voltage  $V_{off}$  for a controllable duration  $t_2 - t_3$ .

The values of  $V_{on}$  and  $V_{off}$  are set by the user, for example, by means of zener diodes, so that  $V_{on} < V_h$  and  $V_{off} > GND$ , with  $V_{on} - GND > V_t$  and  $V_h - V_{off} > V_t$ , 25 where  $V_t$  is the threshold voltage of the controlled IGBT, the IGBT source being grounded.

Advantageously, the gates of transistors 10 and 18 are interconnected, whereby transistors 10 and 18 can be activated or deactivated together by means of a single control signal.

30 Fig. 3 shows a device such as shown in Fig. 1 in which an embodiment of circuit breakers 14 and 16 has been shown in detail.

Circuit breaker 14 comprises a buffer circuit 14', the output terminal of which

can take three states: 1 or 0 according to whether its input terminal is at 1 or 0 or if a control terminal receiving signal S14 is at 1 (off circuit breaker), and a high-impedance state if the control terminal receiving signal S14 is at 0 (on circuit breaker).

Switch 16 comprises a P-channel MOS transistor 36 having its source connected to the control terminal of the Darlington assembly and having its drain connected to the anode of diode D1. The gate of transistor 36 is connected via a resistor 38 to the drain of a P-channel MOS transistor 40. The source of transistor 40 is connected to voltage Vh. The gate of transistor 40 and is connected to the gate of transistor 4, so that transistor 40 forms a current mirror with transistor 4. The gate of transistor 36 is also connected to the anode of a zener diode 42 having its cathode connected to the anode of a zener diode 44 having its cathode connected to the control terminal of the Darlington assembly. The gate of transistor 36 is further connected to the anode of a diode 46 having its cathode connected to the control terminal of the Darlington assembly, and to the cathode of a diode 48 having its anode connected to the drain of transistor 40. A diode 50 has its anode connected to the drain of transistor 40 and its cathode connected to the drain of an N-channel MOS transistor 52 having its source connected to ground GND. The gate of transistor 52 is connected to block 30, for example, to receive control signal S16 illustrated in Fig. 2.

When signal S16 is at 1, transistor 52 is activated and draws the drain of transistor 40 substantially to ground. The gate voltage of transistor 36 is drawn to ground (said gate being connected to the drain of transistor 40 via resistor 38 which conducts no current as long as no current is conducted by zener diodes 42, 44). As seen previously, when the voltage of the output terminal increases, the source voltage of transistor 36, equal to the output voltage plus two diode threshold voltages Vbe, also increases. When  $Vt - Vgs > 0$ , where Vt and Vgs are respectively the threshold voltage and the gate-source voltage of transistor 36, transistor 36 is activated. Switch 16 is then on. The gate voltage of transistor 36 is limited to  $Vh - 2Vz$ , where Vz is the zener voltage of diodes 42 and 44. Voltage  $2Vz$  is selected to protect the gate of transistor 36 while guaranteeing a low resistance Ron of transistor 36. It should be noted that the device will operate even if the source-gate voltage of transistor 36 does not reach  $2Vz$ .

When signal S16 is at 0, transistor 52 is inactive, the current conducted by transistor 40 is provided to the control terminal of the Darlington assembly via diodes 48

and 46, the gate of transistor 36 is at a higher voltage than its source, and transistor 36 is deactivated. Circuit breaker 16 is then off. The size of transistor 40 is selected to provide a current capable of rapidly charging the gate of transistor 36 when signal S16 switches from 1 to 0, and this rapidly turns off circuit breaker 16, with a reasonable power consumption. Diode 48 enables getting rid of the time constant which would otherwise be introduced by resistor 38.

Diode 50 blocks the way of the current when the voltage of terminal OUTH becomes negative (when voltage VI is negative). In the absence of this diode, a current would then flow via the intrinsic diode (not shown) located between the source and the drain of transistor 52, and diodes 48 and 46, and would supply the Darlington assembly in undesirable fashion.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the control device according to the present invention has been shown as comprising both a circuit for setting to the high level and a circuit for setting to the low level according to the present invention, respectively enabling introduction of a stage at the rise and at the fall of the control voltage, but those skilled in the art will easily adapt the present invention to a control device only comprising a circuit for setting to the high level or a circuit for setting to the low level according to the present invention, for example, to introduce a stage at the rise only or at the fall only of the control voltage.

The present invention has been described in relation with the control of an IGBT, but it will easily apply to the control of any other voltage-controlled switch, for example, a MOSfet power transistor.

The present invention has been described in relation with a device providing a voltage control signal stopping as it is rising at a voltage stage Von and as it is falling at a voltage stage Voff but those skilled in the art will easily adapt the present invention to a device providing a voltage control signal stopping at a plurality of stages as it is rising and/or as it is falling, for example, by providing voltages Von and/or Voff that can take a plurality of values.

The present invention has been described in relation with a structure comprising specific elements, but those skilled in the art will easily replace the described elements with equivalent elements. As an example, the described MOS transistors may be of

DMOS or VDMOS type. Similarly, resistor 26 may be made of polysilicon or in the form of a so-called "diffused P" resistor, the substrate of which will be left floating. The Darlington assembly may comprise, as shown, transistors having their emitters connected to the output terminal via resistors, or comprise transistors having their emitters directly connected to the output terminal. The three-state buffer circuit may also be replaced with a three-state inverter circuit receiving an inverted control signal. Further, the two transistors of the Darlington assembly may be confounded in a single bipolar transistor.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention.

10 Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is: